Lattice Semiconductor Corporation™

ispGAL16Z8

In-System Programmable Generic Array Logic™

FEATURES

- **IN-SYSTEM-PROGRAMMABLE — 5-VOLT ONLY**
  - **Change Logic "On the Fly" (in milliseconds)**
  - **Nonvolatile E² Technology**
- **DIAGNOSTICS MODE FOR CONTROLLABILITY AND OBSERVABILITY OF SYSTEM LOGIC**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **20 ns Maximum Propagation Delay**
  - **Fmax = 41.6 MHz**
  - **90mA MAX I_{CC}**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **Maximum Flexibility for Complex Logic Designs**
  - **Programmable Output Polarity**
  - **Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **24-PIN 300-MIL DIP, AND 28-LEAD PLCC PACKAGING**
- **MINIMUM 10,000 ERASE/WRITE CYCLES**
- **DATA RETENTION EXCEEDS 10 YEARS**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **APPLICATIONS INCLUDE:**
  - **Reconfigurable Interfaces and Decoders**
  - **Copy Protection and Security Schemes**
  - **"Soft" Hardware (Generic Systems)**
  - **RFT™ (Reconfiguration For Test)**
  - **Proprietary Hardware/Software Interlocks**

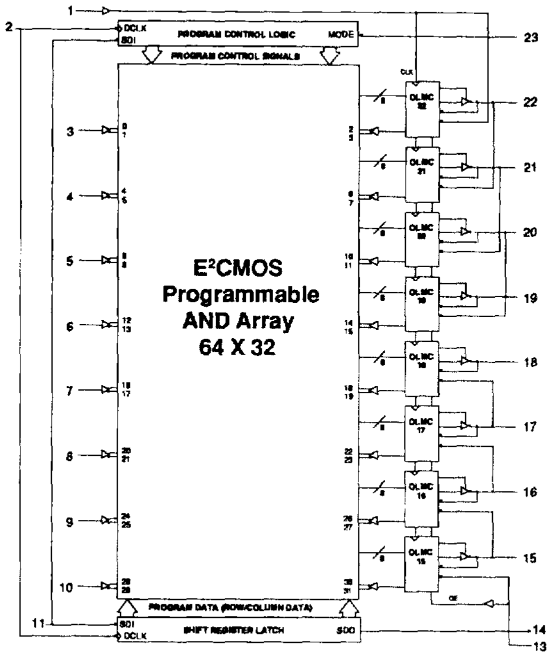
DESCRIPTION

The Lattice ispGAL®16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system programmablitiy and real time, in-system diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage internal programming control signals. Using Lattice's proprietary UltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin ispGAL16Z8 is architecturally and parametrically identical to the 20-pin GAL®16V8, but includes 4 extra pins to control in-system programming. These extra pins are: data clock (DCLK), serial data in (SDI), serial data out (SDO), and mode control (MODE). These pins are not associated with normal logic functions and are typically used for programming and for diagnostics. Additionally, this 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

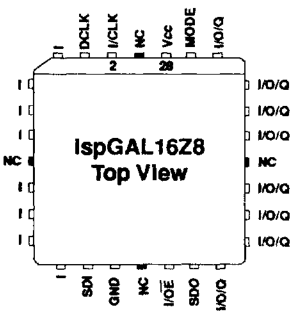
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of the GAL devices . A security circuit is built-in, providing proprietary designs with copy protection.

FUNCTIONAL BLOCK DIAGRAM

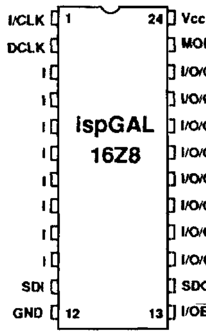


PIN DIAGRAMS

Chip Carrier



DIP



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April 1990

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} .... –.5 to +7V
Input voltage applied .... –2.5 to V_{CC} +1.0V
Off-state output voltage applied .... –2.5 to V_{CC} +1.0V
Storage Temperature .... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress-only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

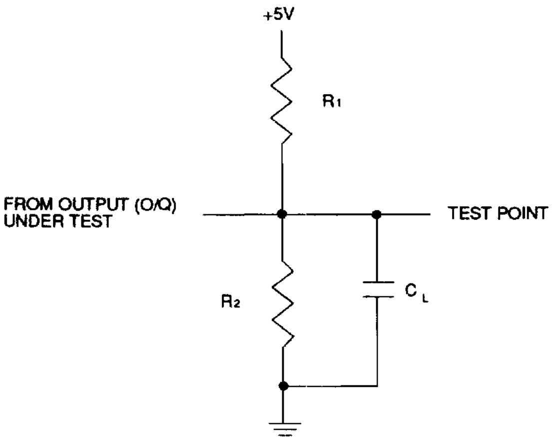
COMMERCIAL		INDUSTRIAL		MILITARY	
R_1	R_2	R_1	R_2	R_1	R_2
200	390	200	390	390	750

AC Test Conditions:

Cond. 1) R_1 per table; C_L = 50pF; R_2 per above table

Cond. 2) Active High $R_1 = \infty$; Active Low R_1 per table; C_L = 50pF; R_2 per above table

Cond. 3) Active High $R_1 = \infty$; Active Low R_1 per table; C_L = 5pF; R_2 per above table



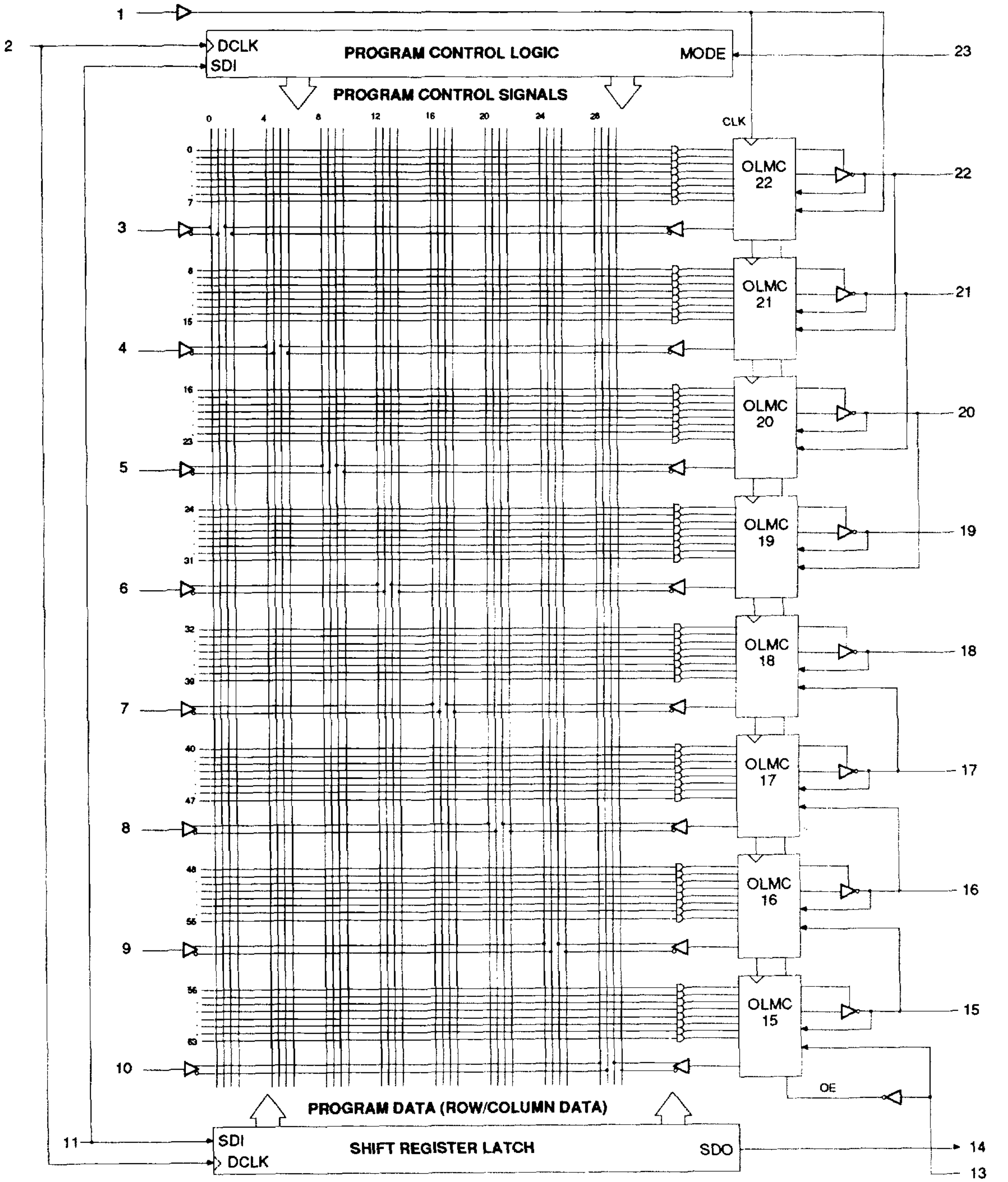
CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

ispGAL16Z8 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — ispGAL16Z8-20L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-20L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS ispGAL16Z8-20L Commercial

Over Recommended Operating Conditions

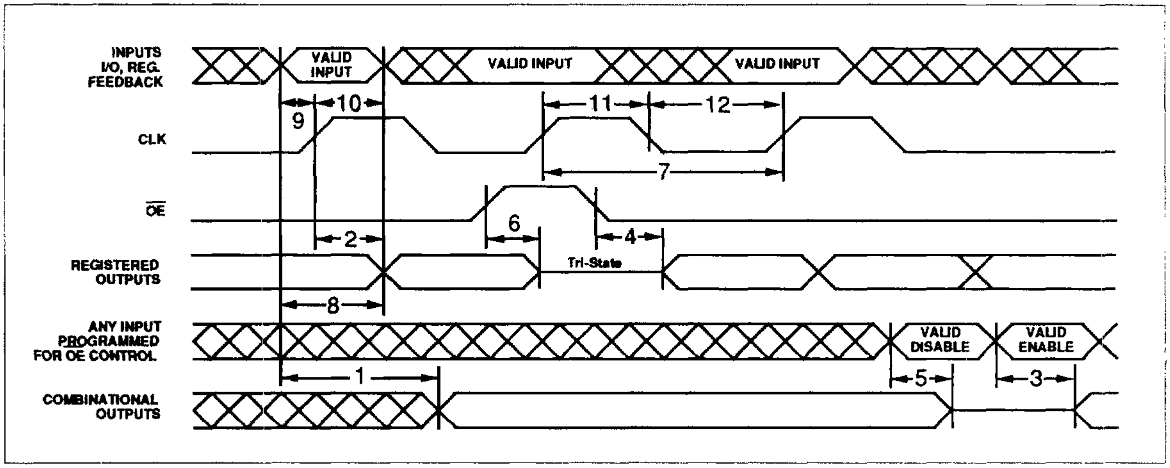
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

AC RECOMMENDED OPERATING CONDITIONS ispGAL16Z8-20L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	41.6	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	12	—	ns
	12	Clock Pulse Duration, Low[2]	—	12	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS ispGAL16Z8-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS ispGAL16Z8-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	-3.2	mA

SWITCHING CHARACTERISTICS — ispGAL16Z8-25L Commercial

Over Recommended Operating Conditions

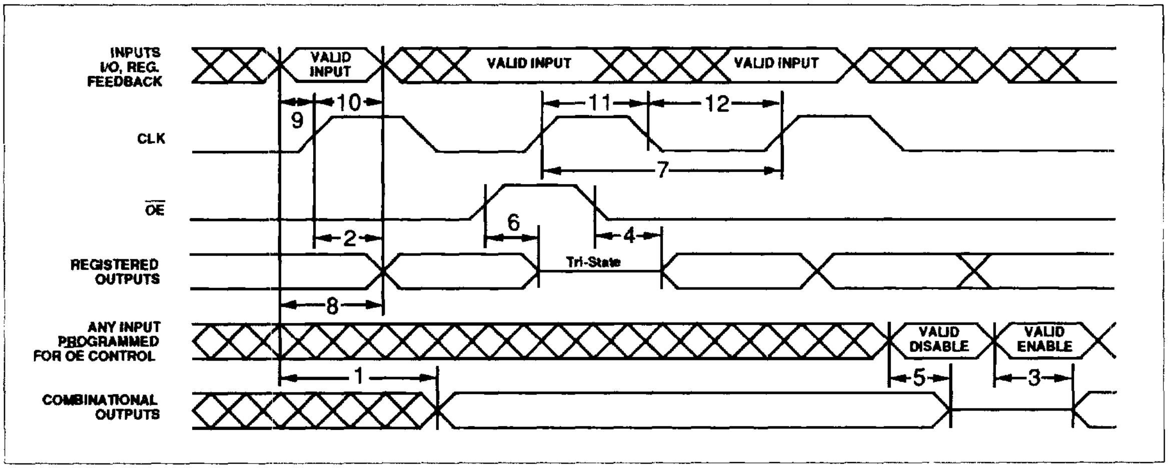
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
t_{co}	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

AC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-25L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback[1] = $1 / (t_{wh} + t_{wl})$	1	0	33.3	MHz
	8	Clock Frequency with Feedback[1] = $1 / (t_{su} + t_{co})$	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High[2]	—	15	—	ns
	12	Clock Pulse Duration, Low[2]	—	15	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



OUTPUT LOGIC MACROCELL (OLMC)

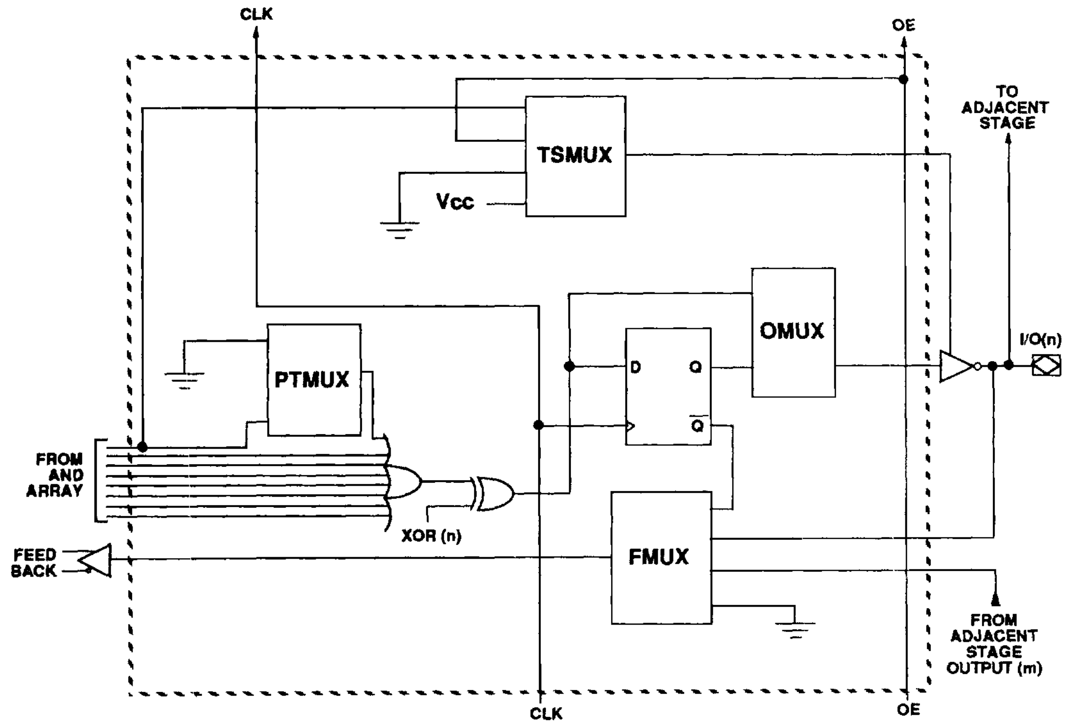
The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

NOTE: See ispGAL16Z8 Programmer's Guide for additional information on in-system OLMC reconfiguration.

There are three OLMC configuration modes possible: registered, complex, and simple. These are illustrated in the diagrams on the following pages. You cannot mix modes, either all OLMCs are simple, complex, or registered (in registered mode the output can be combinational or registered).

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable is connected to all registered outputs; or a product term can be used to provide individual output enable control for combinational outputs in the registered mode or combinational outputs in the complex mode. There is no output enable control in the small mode. The output logic macrocell provides the designer with maximum output flexibility in matching signal requirements, thus providing more functionality than possible with existing 20-pin PAL® devices.

The six valid macrocell configurations, two configurations per mode, are shown in each of the macrocell equivalent diagrams. Pin and macrocell functions are detailed in the following diagrams.



ispGAL®16Z8 Output Logic Macrocell(n)

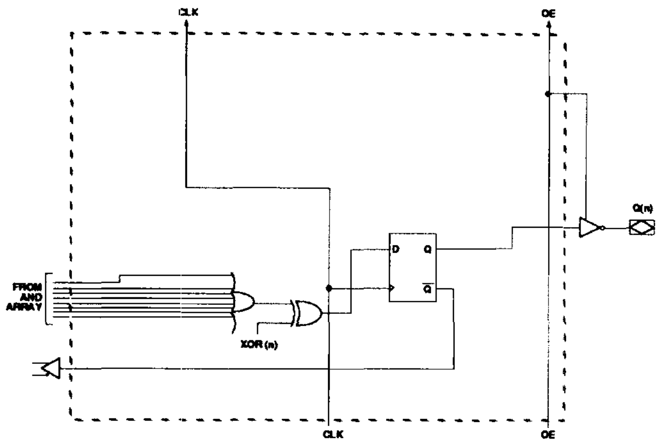
REGISTERED MODE

In the Registered architecture mode macrocells are configured as dedicated, registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and $\overline{OE}$ control pins. Any macrocell can be configured as registered or I/O. Up to 8 registers or up to 8 I/O's are possible in this mode. Dedicated input or output functions can be implemented as sub-sets of the I/O function.

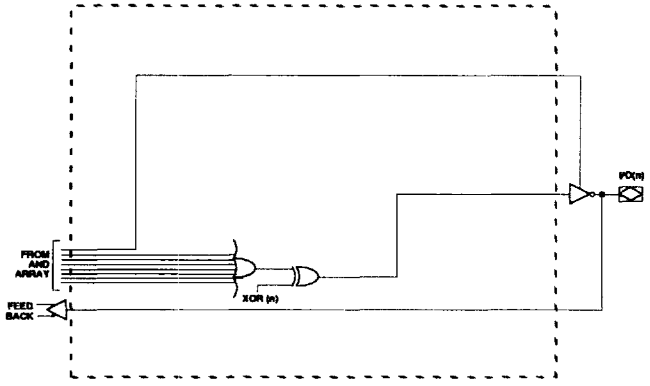
Registered outputs have 8 data product terms per output. I/O's have 7 data product terms per output.



Registered Output with Programmable Polarity

NOTES:

- All macrocells can be individually configured to this function.
- Polarity of the register input is programmable on a macrocell by macrocell basis.
- Feedback into the AND array is from the $\overline{Q}$ signal of the register with active low and active high feedback paths provided.
- Registered macrocells have common clock (pin 1) and common $\overline{OE}$ (pin 13)



Combinational Input/Output with Programmable OE and Polarity

NOTES:

- All macrocells can be individually configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- All macrocells have active high and active low feedback of the output buffer and/or device pin data into the AND array.
- When all 8 macrocells are configured into the I/O function the CLK and $\overline{OE}$ pins serve no valid logic function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

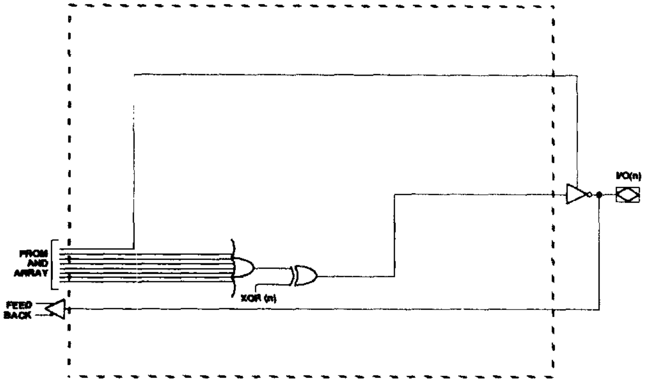
COMPLEX MODE

In the Complex architecture mode macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

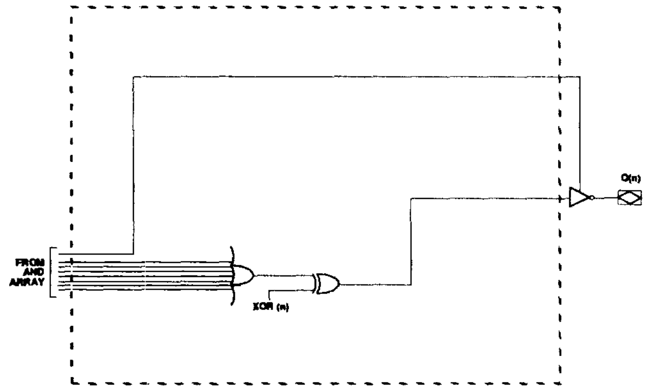
Up to 6 I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as sub-sets of the I/O function. The two "outboard" macrocells do not have input capability. Designs requiring 8 I/O's can be implemented in the Registered mode.

All macrocells have 7 data product terms per output. One product term is used for programmable OE control. Pins 1 and 13 are always available as data inputs into the AND array.



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- The outer most macrocells (pins 15 & 22) cannot perform this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- Each macrocell has active high and active low feedback of the output buffer and/or device pin data into the AND array.



Combinational Output with Programmable OE and Polarity

NOTES:
- The two outer most macrocells (pins 15 & 22) are permanently configured to this function when in the Complex mode.
- The other 6 macrocells can emulate this mode by not using the feedback data as a data input to the array.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every ispGAL16Z8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

TC CELL

The ispGAL16Z8 is equipped with a TC (Tri-state Control) cell which allows output driver state control during in-system programming and/or diagnostic mode. In the default setting (logic 1), this cell causes the output state (logic 1, logic 0, or tri-state) to be latched upon entering the programming/diagnostic mode. In the tri-state setting (logic 0), this cell causes all outputs to tri-state upon entering the programming/diagnostic mode.

NOTE: Refer to the ispGAL16Z8 Programmers Guide for additional information on TC cell programming and functionality.

SECURITY CELL

A security cell is provided with every ispGAL16Z8 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased.

NOTE: Refer to the ispGAL16Z8 Programmers Guide for additional information on the Bulk Erase procedure.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break any feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next-state conditions.

The ispGAL16Z8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any desired state condition can be forced for test sequencing.

NOTE: Refer to the ispGAL16Z8 Programmers Guide for additional information on registered oriented diagnostic preload.

LATCH-UP PROTECTION

ispGAL16Z8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

ispGAL16Z8 devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, require much less drive current than traditional bipolar devices. This allows for a greater fan out from the driving logic.

ispGAL16Z8 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

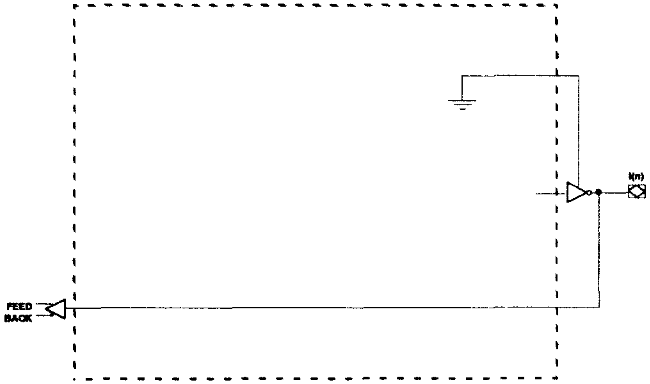
SIMPLE MODE

In the Simple architecture mode pins are configured as dedicated inputs or as dedicated, always active, combinational outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 16P6 devices with many permutations of generic polarity output or input choices.

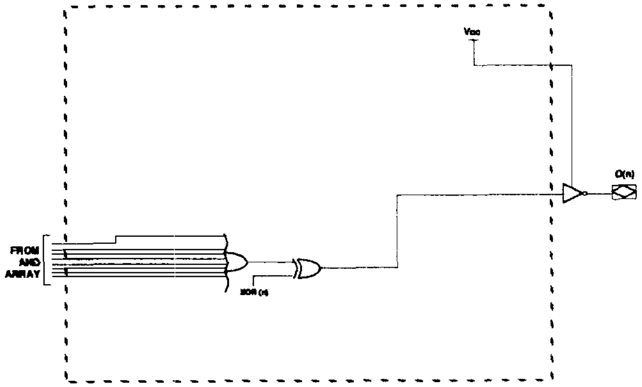
All ouputs are associated with 8 data product terms. In addition, each output has programmable polarity.

Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 15 &16) cannot be used in the input configuration.



Dedicated Input Mode

NOTES:
- The "center" two macrocells (18 & 19) cannot be configured to this function.

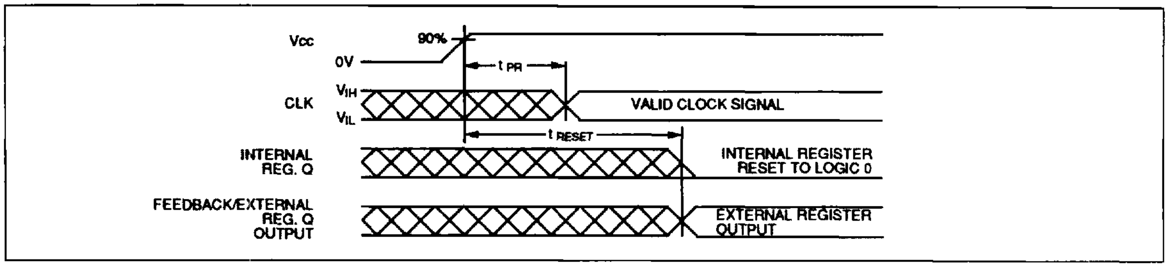


Dedicated Combinational Output with Programmable Polarity

NOTES:
- All Macrocells can be configured to this function. The "center" macrocells (pins 18 & 19) can only be configured to this function when in the Simple mode.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- The outputs can also be permanently programmed tri-stated.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

POWER-UP RESET



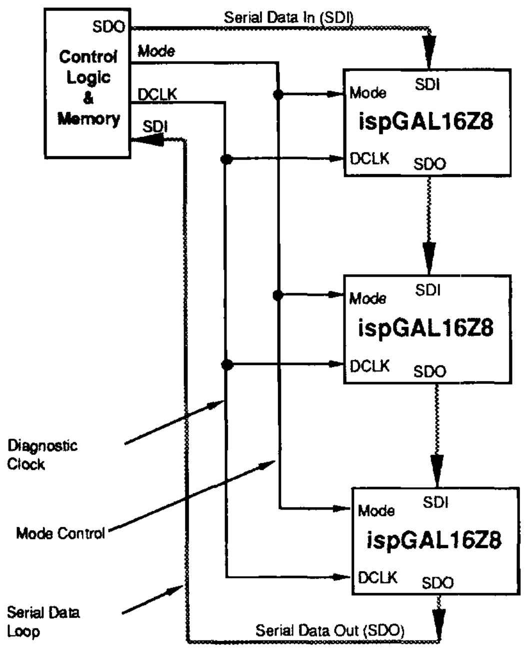
Circuitry within the ispGAL16Z8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the ispGAL16Z8. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

SERIAL PROGRAMMING: LOOP OPERATION

The following figure illustrates a simplified block diagram of a microprocessor system containing three (3) ispGAL16Z8 devices. These devices have been "daisy chained" together to form a serial programming/diagnostic loop. In this configuration, the data bit rate and the DCLK clock frequency are the same. A programming and/or diagnostic bit stream may be shifted through all three (3) devices at the maximum DCLK clock frequency. The ispGAL16Z8 data cells are not dynamic. In other words, there is no minimum DCLK clock frequency.

In this configuration, only four (4) wires are required to access and control an unlimited number of devices. All the functions associated with reprogrammable logic devices are available via this 4-wire interface. An important benefit offered by the ispGAL16Z8 is RFT (Reconfiguration For Test) capability. RFT is a concept pioneered and developed by Lattice Semiconductor. RFT, in brief, is the process of reprogramming Lattice ispGAL devices, in-circuit, to serve as on-board diagnostic test vector drivers and/or receivers. Any pin associated with an OLMC (Output Logic Macro-Cell) can be configured via the 4-wire serial interface to serve as an output or an input. Elementary test vector sequencing or driver/receiver control can be achieved by patterning portions of the ispGAL16Z8 to serve as a micro-control state-machine.



Typical ispGAL16Z8 Daisy Chain

ispGAL16Z8 PROGRAMMERS GUIDE

The ispGAL16Z8 Programmers Guide contains complete information on the use of the serial programming and diagnostic capability of the ispGAL16Z8 device. The information provided in this datasheet <u>is insufficient</u> to properly design circuitry to control the device. The information is presented here only for reference and conceptual design evaluation. The guide can be requested from the Applications Engineering department at the factory.